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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
ARNOLD, ADAM

ART UNIT	PAPER NUMBER
2697	6

DATE MAILED: 03/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,956	PETHER ET AL.	
	Examiner	Art Unit	
	Adam Arnold	2697	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/3/03* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 13-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 13-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

The examiner acknowledges the receipt and entry of the applicant's amendment.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 20 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee, U.S. Patent No. 5,214,753. Referring to claim 1, Lee discloses a graphics display apparatus (col. 4, line 36) comprising a bus having a first address range and a second address range (col. 22, lines 1-8), a plurality of registers within the first address range configured to store an x and y coordinate of a pixel to be drawn (col. 8, lines 19-23), a memory within the second address range (col. 22, lines 8-10), a calculation circuit to determine an address for storage of data corresponding to the pixel in dependence on x and y coordinates (col. 17, line 59), and a control circuit for writing the data into said memory at the appropriate address (col. 18, line 30, and Figures 1A, no. 33).

Referring to claim 3, Lee discloses the apparatus of claim 1, further comprising a clipping circuit which serves to determine which coordinates fall outside of a particular threshold. See col. 15, line 24.

Referring to claim 20, Lee discloses a system for generating a region of graphics on a display as described fully in claim 1 above. The remarks directed to claim1 above, apply equally to claim 20. The apparatus of Lee performing the steps is recited in the claim.

Referring to claim 30, The remarks directed to claim1 above, apply equally to claim 30.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Ashburn, U.S. Patent No. 5,651,106. Referring to claim 4, Lee discloses the graphics apparatus of claim 3. See 102 rejection above. Lee does not expressly teach that the control circuit responds to the clipping unit to inhibit writing data to the memory address. Ashburn discloses a control circuit attached to a clipping unit to inhibit writing data to memory. See Ashburn, col. 8, lines 29-31. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the control circuit responding to the clipping unit to inhibit writing data to the memory address. One of ordinary skill in the art would have been motivated to do this to increase performance levels in graphics systems. Further, both Lee (col. 15, line 24) and Ashburn disclose clipping and Ashburn is relied upon to show common specifics for the clipping that Lee is silent on.

Referring to claim 5, Lee discloses the graphics apparatus of claim 3. See 102 rejection above. Lee does not expressly teach that the control circuit responds to the clipping unit to prevent calculation of an address in memory. Ashburn discloses a control circuit attached to a clipping unit to prevent calculation of an address in memory. See Ashburn, col. 8, lines 29-31.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the control circuit responding to the clipping unit to prevent calculation of an address in memory. One of ordinary skill in the art would have been motivated to do this to increase performance levels in graphics systems.

5. Claims 6 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Foley. Referring to claim 6, Lee discloses the graphics apparatus of claim 3. See 102 rejection above. Lee does not expressly teach that the data is discarded when at least one of the x and y coordinates fall outside the predetermined clipping limits. However, Lee refers to Foley for a complete description of clipping techniques. Foley teaches that pixels outside the clipped region are not processed. "The primitive is also *clipped* to the clip rectangle; that is pixels belonging to the primitive that are outside the clip region are not displayed." See Foley, p. 71, lines 22-23. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to not process pixels outside the clipping region. One of ordinary skill in the art would have been motivated to do this because the general purpose of clipping is to select the data set to process and to not process the clipped off data which allows for both quicker processing and more accurate displays. Further, similar to the reasoning provided in the proceeding paragraph (4), Foley provides common details for clipping.

Referring to claim 21, Lee in view of Foley discloses a system for generating a region of graphics on a display by comparing coordinates with clipping limits as described in claim 20 and 6 above. The remarks directed to claims 6 and 20, above, apply equally to claim 21.

6. Claims 7 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Krenik, U.S. Patent No. 5,699,087. Referring to claim 7, Lee discloses the graphics

apparatus of claim 2. See 102 rejection above. Lee does not teach a 1st register mapped to a 1st and 2nd location in memory and a 2nd register mapped to a 3rd and 4th location in memory. Krenik teaches a memory circuit having a plurality of memory locations for storing an item of data. See col. 10, line 30. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a 1st register mapped to a 1st and 2nd location in memory and a 2nd register mapped to a 3rd and 4th location in memory. One of ordinary skill in the art would have been motivated to do this because this type of memory accessing procedure is conventional as shown by Krenik.

Referring to claim 22, Lee in view of Foley discloses a system for generating a region of graphics on a display by mapping the registers to multiple memory locations as described in claim 20 and claim 7 above. The remarks directed to claims 7 and 20, above, apply equally to claim 22.

7. Claims 8-10 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Krenik, further in view of Chiu, U.S. Patent No. 5,796,391. Referring to claim 8, Lee in view of Krenik discloses the graphics apparatus of claim 7. See 103 rejection above. Lee does not teach an address decoder for monitoring the memory locations. Chiu teaches an address decoder attached to a control unit. See col. 3, line 45 and Figure 2, nos. 122 and 206. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have an address decoder for monitoring memory locations. One of ordinary skill in the art would have been motivated to do this because address decoders are conventionally used to access memory locations and because it allows the locations in the registers to be translated into a memory location. Further, the references show storing/retrieving data from memory and, to do

so, an address is needed. The conventional way to do this is using an address decoder as shown by Chiu.

Referring to claim 9, Lee in view of Krenik, further in view of Chiu discloses the graphics apparatus of claim 8. See 103 rejection above. Lee does not teach a control circuit configured to control address registers in response to an address decoder. Chiu teaches a control circuit configured to control address data in response to an address decoder. See col. 3, line 46. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a control circuit configured to control address registers in response to an address decoder. One of ordinary skill in the art would have been motivated to do this to provide a load signal on the data outputs, as well as the reasons given previously.

Referring to claim 10, Lee in view of Krenik, further in view of Chiu discloses the graphics apparatus of claim 9. See 103 rejection above. Lee does not teach calculating an address for the pixel based on an X coordinate being sent to one of a 1st and 2nd memory locations and a Y coordinate being sent to one of a 3rd and 4th locations. Krenik teaches a memory circuit having a plurality of memory locations for storing an item of data. See col. 10, line 30. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to calculate an address for the pixel based on an X coordinate being sent to one of a 1st and 2nd memory locations and a Y coordinate being sent to one of a 3rd and 4th locations. One of ordinary skill in the art would have been motivated to do this to reduce the time required to access data, as well as the reasons given previously. See Krenik, col. 2, line 43

Referring to claim 23, Lee in view of Krenik, further in view of Chiu discloses a system for generating a region of graphics on a display by monitoring multiple memory locations as

described in claim 22 and claim 8 above. The remarks directed to claims 8 and 22, above, apply equally to claim 23.

Referring to claim 24, Lee in view of Krenik, further in view of Chiu discloses a system for generating a region of graphics on a display by using multiple memory addresses as described in claim 23 and claim 10 above. The remarks directed to claims 10 and 23, above, apply equally to claim 24.

8. Claims 11, 13, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Prouty, U.S. Patent No. 5,986,658. Lee does not teach a style table for storing data corresponding to a predetermined style for the pixel, or a style counter for indexing the data in the style table. Prouty teaches a line style array for storing line style pattern features and a line style feature pixel counter. See Figure 2, elements 211 and 217. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a style table for storing data corresponding to a predetermined style for the pixel and a style counter for indexing the data in the style table. One of ordinary skill in the art would have been motivated to do this to provide for drawing complex line styles in real time. See Prouty, col. 1, lines 4-9. Further, both references are directed to the generation and use of raster computer graphics (see col. 1, lines 9-15 of Lee and lines 1-2 of the Prouty abstract). Thus, Prouty simply provides details of the generation of a specific type of graphic, the type being more generally described and used by Lee.

Referring to claim 13, Lee in view of Prouty discloses the graphics apparatus of claim 11. See 103 rejection above. Lee does not teach a style table configured to store a non-repeating bit pattern up to a predetermined length. Prouty teaches an array large enough to handle line style

pattern features. See Prouty, col. 7, line 29. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a style table configured to store a non-repeating bit pattern up to a predetermined length. One of ordinary skill in the art would have been motivated to do this to provide for different size bit patterns.

Referring to claim 25, Lee in view of Prouty discloses a system for generating a region of graphics on a display by utilizing style data as described fully in claim 20 and claim 11 above. The remarks directed to claims 11 and 20, above, apply equally to claim 25.

Referring to claim 26, Lee in view of Prouty discloses a system for generating a region of graphics on a display as described in claim 25 above. Lee does not disclose selecting a color for the pixel to be drawn dependent on the style data signal. Prouty discloses that in a preferred embodiment of their invention, the style array records color information for the line. See col. 5, line 19. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a style table record color information for the pixel. One of ordinary skill in the art would have been motivated to do this to record accurate information regarding the graphics display as well as the reasons above.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Prouty, further in view of Krenik and Chiu. Lee in view of Prouty discloses the graphics apparatus of claim 12. See 103 rejection and claim objections above. Lee does not teach a 1st register mapped to a 1st to 4th location in memory and a 2nd register mapped to a 5th to 8th location in memory or an address decoder for monitoring the locations. Krenik teaches a memory circuit having a plurality of memory locations for storing an item of data. See col. 10, line 30. Chiu teaches an address decoder attached to a control unit. See col. 3, line 45 and Figure 2, nos. 122

and 206. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize Krenik's plural memory locations and Chiu's address decoder with the graphics display apparatus. One of ordinary skill in the art would have been motivated to do this to reduce the time required to access data as well as the reasons given above. See Krenik, col. 2, line 43. Additionally, see the remarks presented above for the reasons for combining the individual references.

10. Claim 15-19 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Ozcelik, Patent Publication No. 2002/0149626. Referring to claim 15, Lee further discloses a register and memory accessible via a bus (col. 18, lines 25-30). Lee does not teach outputting a word address corresponding to the address location in memory and a bit address representing a position of the pixel data within a word. Ozcelik teaches outputting a word address corresponding to the address location in memory and a bit address representing a position of the pixel data within a word. See paragraph 47. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to output a word address corresponding to the address location in memory and a bit address representing a position of the pixel data within a word. One of ordinary skill in the art would have been motivated to do this to reduce complexity and increase flexibility in defining displays. See Ozcelik, paragraph 8. Further, Ozcelik provides the details of addressing memory for storage/retrieval of data such as done in Lee.

Referring to claim 16, Lee in view of Ozcelik discloses the graphics apparatus described in claim 15. See 103 rejection above. Lee further discloses a second register for storing pixel data and a multiplexer for writing data to a register. See Lee, col. 23, line 60.

Referring to claim 17, Lee in view of Ozcelik discloses the graphics apparatus described in claim 16. See 103 rejection above. Lee further discloses a multiplexer which combines data for two or more pixels. See Lee, col. 23, line 60.

Referring to claim 18, Lee in view of Ozcelik discloses the graphics apparatus described in claim 17. See 103 rejection above. Lee further discloses a comparator connected to a calculation circuit for receiving and comparing word addresses. See Lee, col. 28, line 11 for alternative embodiments.

Referring to claim 19, Lee in view of Ozcelik discloses the graphics apparatus described in claim 18. See 103 rejection above. Lee further discloses a control circuit which combines the data for the pixels in response to a receipt of the same address signal. See Lee, col. 23, line 66.

Referring to claim 27, Lee in view of Ozcelik discloses a system for generating a region of graphics on a display storing pixel data in a memory word as described fully in claim 20 and claim 17 above. The remarks directed to claims 17 and 20, above, apply equally to claim 27.

Referring to claim 28, Lee in view of Ozcelik discloses a system for generating a region of graphics on a display combining pixels to be drawn dependent on a word address as described fully in claim 20 and claim 15 above. The remarks directed to claims 15 and 20, above, apply equally to claim 28.

Referring to claim 29, Lee in view of Ozcelik discloses a system for generating a region of graphics on a display utilizing a comparator as described fully in claim 20 and claim 18 above. The remarks directed to claims 18 and 20, above, apply equally to claim 29.

Response to Arguments

11. Applicant's arguments, see page 24, line 12, filed February 3, 2003, with respect to the objections to claims 12-14 have been fully considered and are persuasive. The objections to claims 12-14 have been withdrawn.

12. Applicant's arguments filed February 3, 2003 have been fully considered but they are not persuasive. Referring to the rejection to claims 1, 3, 20 and new claim 30, the applicant states the amendments have obviated the previous rejection in that Lee does not disclose or suggest every element as arranged in the claims. It is the examiner's position that Lee does disclose every element as arranged in the claims (see remarks above with respect to claims 1, 3, 20 and 30 above) and the claims are hereby rejected.

In response to applicant's argument (on the top of page 32) that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

In response to applicant's argument that there is no suggestion to combine the references (for claims 4-11, 13-19 and 21-29), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988 and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, there is sufficient motivation found in the references and in knowledge available to one of ordinary skill in the art to combine the references and the examiner believes the motivations presented in the first action to be sufficient.

However, in response to applicant's remarks additional reasoning has been supplied in the above rejections. The rejections to these claims stand.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Adam Arnold** whose telephone number is **703-305-8413**. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso, can be reached at (703) 305-3885.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).